Claim 1 (Presently Amended) A multi-layered semiconductor device characterized in that a film-like semiconductor package incorporating therein a semiconductor chip is disposed in a package accommodation opening of a circuit pattern layer to form a circuit board, said circuit pattern layer comprises a substrate, a circuit pattern formed on the substrate, and said package accommodation opening, and a plurality of such circuit boards are layered together to electrically connect said circuit patterns of the respective circuit boards with each other,

wherein the electrical connection between the circuit patterns on the respective circuit boards is performed via a low melting point metal filled in a ~~through hole~~ through-hole formed in the semiconductor package or the circuit board, and the electric connection between the semiconductor package and a circuit pattern layer accommodating the semiconductor package is performed by connecting an extension of the circuit pattern, formed on the semiconductor package to project outside the package, with an electrode pad of the circuit pattern layer.

2. (Original) A multi-layered semiconductor device as defined by claim 1, wherein every adjacent circuit board is bonded to another with an insulation adhesive except for an electrically connected portion.

3. (Canceled)

4. (Original) A multi-layered semiconductor device as defined by claim 1, wherein the electrical connection between the circuit patterns on the respective circuit boards is performed by connecting an extension of the circuit pattern into a hole formed in

the semiconductor package or the circuit board with an electrode pad of the circuit pattern in the other circuit board positioned beneath the former circuit board.

5-10. (Canceled)

11. (Presently Amended) A multi-layered semiconductor device formed of a plurality of circuit boards layered together, each circuit board comprising an insulation substrate, a semiconductor chip incorporated in the substrate, a circuit formed on the surface of the substrate and connected to the semiconductor chip, characterized in that a lead extending from one of the circuit ~~board~~ boards of the plurality of circuit boards is bonded to a circuit on another circuit board disposed beneath the former circuit board to establish an interlayer connection, said lead extending through a through-hole in the insulation substrate of the former circuit board, wherein at least one of the plurality of circuit boards incorporates a plurality of semiconductor chips therein.

12. (Canceled)

13. (Original) A multi-layered semiconductor device as defined by claim 11, wherein every adjacent circuit board is bonded to another with an insulation adhesive.

14. (Original) A multi-layered semiconductor device as defined by claim 11, wherein the semiconductor chip is accommodated in a through-hole formed in the insulation substrate of at least one of the plurality of circuit boards, and is electrically connected to the circuit of the circuit board by a beam lead bonding.

15. (Original) A multi-layered semiconductor device as defined by claim 11, wherein the semiconductor chip is accommodated in a through-hole formed in the insulation substrate of at least one of the plurality of circuit boards, and is electrically connected to the circuit of the circuit board and the semiconductor chip by a flip-chip connection.

16. (Previously Presented) A multi-layered semiconductor device as defined by claim 11, wherein the circuit on the circuit board is electrically connected, by means of a low melting point metal filled in a through-hole provided in the insulation substrate of the circuit board, to a circuit on an adjacent circuit board to establish an interlayer connection.

17. (Canceled)

18. (Canceled)